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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/740,469	12/22/2003	Kouichi Takagi	118153	3615
25944	7590	03/06/2006	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			NGUYEN, HOA CAO	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-6, in the reply filed on 1/12/06 is acknowledged. The traversal is on the ground(s) that the subject matter of all claims is sufficiently related that a thorough search for the subject matter of any one group of claims would encompass a search for the subject matter of the remaining claims.

This is not found persuasive because Inventions II (claim 7) and I (claims 1-6) are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP j 806.05(9)). In the instant case, the product as claimed can be made by another and materially different process such as to bridge the inner surface of the conductor layer, a conductive film can be formed with conductive adhesive glue instead of soldering. Furthermore, applicants clearly admitted that the product as claimed could be made by various methods (see specification, page 10, second paragraph).

The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Reference character 72 in figure 12. Corrected drawing sheets in

compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. Figures 13A and 13B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Downie et al. (US 5471368).

Regarding claim 1, as shown in figures 4 and 5, Downie et al. disclose a control circuit board 110 (a module, see column 4, line 4-5) comprising:

(a) A connecting portion to be connected to an external circuit 20 (a substrate, see column 4, line 21),

(b) the connecting portion is configured such that an end portion of the control circuit board is formed with a cut 50 (cutting via, see column 4, lines 12-13) which is opened sideways (as shown in figure 4),

(c) the connecting portion is coated with a conductor layer 53 (electrically conductive material, see column 4, line 8) in such a manner that an inner side surface of the cut is covered with the conductor layer 53 (electrically connected to pad 55),

(d) the conductor layer is inherently connected to a circuit that is incorporated in the control circuit board (the conductive pads 55 are for circuit connections).

It is noticed that the teachings from the reference art centering about an edge connection of a substrate are not limited to a direct chip attach module (as a preferred embodiment and for illustration purpose). It is understood that the substrate 110/20 can be any electrical circuit board/layer/module such that the teachings are usable and applicable, and a control means and/or other function means are the ability to so perform.

Regarding claim 2, as shown in figure 5, Downie et al. disclose a circuit structural body comprising:

(a) A plurality of bus bars 40 (circuit lines, see column 3, line 58) that are part of a power circuit (considering the circuit pattern formed on substrate 20 is a power circuit pattern);

(b) the power circuit (formed on substrate 20) are bonded to a surface of a control circuit board 110 in a state that the bus bars 40 are arranged approximately in the same plane (as shown in the figure);

(c) as described in claim 1 above, the control circuit board 110 including a connecting portion inherently to be connected to an external circuit (a circuit connecting to the circuit lines 40, the connecting portion is configured such that an end portion of the control circuit board is formed with a cut 50 which is opened sideways and is coated with a conductor layer 53 in such a manner that an inner side surface of the cut is covered with the conductor layer, the conductor layer is connected to a circuit that is inherently incorporated in the control circuit board;

(d) a particular one of the bus bars 40 is electrically connected to the circuit incorporated in the control circuit board by soldering 65 (solder joint fillet, see column 4, line 24) in which solder is supplied so as to bridge an inner circumferential surface of the conductor layer 53 of the control circuit board and a surface 60 (connection pad, see column 4, line 24) of the particular bus bar 40 in a state that a coating portion of the conductor layer is laid on the particular bus bar 40 (as shown in the figure).

Regarding claim 3, as shown in figure 5 and 1A, Downie et al. disclose a IC chip 30 (considering the IC chip 30 as a switching element - A multi-FET IC chip is conventionally known in the art) is provided in the power circuit (pin 31 can penetrate through substrate 110 and connect a substrate or circuit layer formed below) including the bus bars, the control circuit board incorporates a control circuit for controlling driving of the switching element, and the switching element is mounted so as to bridge the bus bar and the control circuit board (since a connecting pin can penetrate through a multilayer circuit board).

Regarding claim 4, as shown in figure 5, Downie et al. disclose a plurality of bus bars 40 project sideways from the control circuit board to serve as terminals to be connected to the external circuit, and at least part of the bus bars to serve as the terminals that are electrically connected to the conductor layers by soldering.

Regarding claim 6, as shown in figure 5, the terminals (formed by bus bar 40) inherently include signal input terminals to which instruction signals are input externally, and the bus bars to serve as the signal input terminals are electrically connected to the conductor layers.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Downie et al. in view of Kasai (US 6116916).

Downie et al. disclose every limitation as shown in claims 2 and 4 above but fail to disclose the bus bars to serve as the terminals that are bent in the same direction that is generally perpendicular to the control circuit board.

Kasai, as shown in figure 1, discloses an electrical connection box comprising bus bars 24 (see abstract) inherently part of a power circuit and a control circuit board 23 (a printed circuit board having electric devices mounted thereon, see column 4, lines 2-3), wherein the bus bars 24 are bent in the same direction that is generally perpendicular to the control circuit board 23 to form a male connector (see column 4, lines 43-45).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings about the forming of a male connector from a bus bar on the board of Downie et al. in order to make a male connector to serve as an input/output port for the board.

Citation of Relevant Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Koshiba (US 6437986) discloses a fuse relay junction block for use in automobiles.

Terashima et al. (US 6452112) disclose an electronic circuit unit useful for portable telephone, etc., and a method of manufacturing the same.

Dishongh et al. (US 20030183420) disclose a circuit board with via through surface mount device contact.

Olzak et al. (US 20020093803) disclose an adapter for plastic-leaded chip carrier (PLCC) and other surface mount technology (SMT) chip carriers.

Okada et al. (US 6534726) disclose a module substrate and method of producing the same.

Kennedy et al. (US 20010032740) disclose a microwave package.

Handforth et al. (US 6061241) disclose a line interface module.

Chiriku et al. (US 6610926) disclose a junction box.

Mizuno et al. (US 6466451) disclose an electric connection box.

Saito et al. (US 6402530) disclose a junction box.

Matsumoto et al. (US 5067905) disclose an electric connection box.

Conclusion

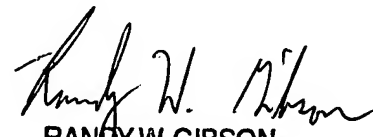
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
2/28/06


RANDY W. GIBSON
PRIMARY EXAMINER